IN THE SPECIFICATION:

Please amend paragraph number **[0001]** as follows:

[0001] This application is a divisional of application Serial No. 10/331,033, filed December 27, 2002, ~~pending,~~ now U.S. Patent 6,703,263, issued March 9, 2004, which is a continuation of application Serial No. 09/901,761, filed July 9, 2001, now U.S. Patent 6,511,868, issued January 28, 2003, which is a continuation of application Serial No. 09/165,754, filed October 2, 1998, now U.S. Patent 6,277,674, issued August 21, 2001.

Please amend paragraph number **[0007]** as follows:

[0007] The present invention generally provides fuses for integrated circuits and semiconductor devices, methods for making the same, methods of using the same, and semiconductor devices containing the same. The semiconductor fuse of the present invention contains two conductive ~~layers~~ layers, an overlying layer and an underlying ~~layer~~ layer, disposed on an insulating substrate. The underlying layer comprises a refractory metal nitride, such as titanium nitride, and the overlying layer comprises tungsten silicide. The semiconductor fuse may be fabricated during manufacture of local interconnect structures containing the same materials.

Please amend paragraph number **[0019]** as follows:

[0019] Next, as shown in Figure 2, silicon nitride layer 8 and pad oxide layer 4 are patterned by any suitable process known in the art, thereby removing undesired portions of silicon nitride layer 8 and pad oxide layer 4 above portions of substrate 2 where field isolation regions 10 will be formed and leaving silicon nitride layer 8a and pad oxide layer 4a. The structure in Figure 2 is illustrated in two ~~portions~~ portions, portion 200 containing the to-be-formed fuse and portion 100 containing the to-be-formed local interconnect ~~structure separated~~ structure, separated by the vertical dotted line. Any suitable patterning process known in the art, such as a photolithographic pattern and etch process, can be used to pattern silicon nitride layer 8 and pad oxide layer 4. For example, a photoresist film can be spun on silicon

nitride layer 8, developed, and portions thereof removed to leave photoresist mask 9 (shown by the dotted line in Figure 1). Using photoresist mask 9, the undesired portions of silicon nitride layer 8 and pad oxide layer 4 are then removed by any suitable anisotropic etching process to obtain silicon nitride layer 8a and pad oxide layer 4a. Photoresist mask 9 may then be removed by any suitable process known in the art which does not attack silicon nitride layer 8a or substrate 2.

Please amend paragraph number **[0033]** as follows:

[0033] Neck portion 30 is that portion of fuse 34 that will blow when subjected to programming or sufficient electrical current. For the preferred dimensions of neck portion 30 above, when a sufficient amount of ~~current~~ current, about 1 to about 25 mA and preferably about ~~5.5 mA~~ 5.5 mA, flows through conductive layer 26, it heats up and melts in neck portion 30, thereby interrupting the current flow. Neck portion 30 blows before terminal portions 28 because, while the same amount of current runs through both, there is less area in neck portion 30. Consequently, the temperature of neck portion 30 is higher than the temperature in terminal portions 28, leading to quicker melting of conductive layer 26 in this region. Reducing the width-to-length ratio of neck portion 30 and changing the material of conductive layer 26 will change the amount of current needed to blow the fuse 34. Tungsten silicide is the preferred material for conductive layer 26 since, when practiced in the present invention, the tungsten silicide requires only about half the electrical current to blow as a polysilicon fuse with similar dimensions. After the fuse is blown by this electrical current, the leakage current of the blown fuse ranges from about 1 to about 10 nA and is preferably less than about 1 nA.